Product Information Sheet

PXDAC4800

1.2 GSPS 4-Channel Arbitrary Waveform Generator

FEATURES

- 4 AC-Coupled or DC-Coupled DAC Channel Outputs
- 14-bit Resolution @ 1.2 GSPS for 2 Channels or 600 MSPS for 4 Channels
- 8-bit Resolution @ 1.2 GSPS for 4 Channels
- 1 Gigabyte DDR2 RAM
- Up to 900 MB/s (sustained) via 8-lane PCI Express Bus
- Based on Analog Devices AD9736 DAC
- Output Ranges from 400mV to 1470mV
- Bandwidth up to 400 MHz (AC-Coupled) or 590 MHz (DC-Coupled)

APPLICATIONS

- Waveform Generation or Playback
- Radar
- Video
- Communications
- Ultrasound
- Automated Testing

OVERVIEW

The PXDAC4800 is an exceptionally high-speed four channel Digital to Analog Conversion (DAC) board which may be used as an Arbitrary Waveform Generator, a waveform playback device, or for generating multiple communication frequency bands. Each DAC can output data at a maximum real rate of 1.2 GSPS at 14-bit for two channels or at 8-bit for four channels, or 600 MSPS at 14-bit for four channels. Each output signal has a bandwidth of up to 400 MHz for AC-Coupled configuration or up to 590 MHz for DC-Coupled configuration. Output waveforms may be “per-trigger” or “continuously looped” from the on-board 1 Gigabyte memory.

The DACs can also be provided with a continuous data stream via the PCI Express (PCIe) bus up to 900 Megabytes per second (MB/s). This PCIe bus rate allows for providing up to 112.5 MSPS addressable bandwidth at full 14-bit resolution for each of the four analog outputs.

The DAC clock source may be selected as either the 1200 MHz or 900 MHz VCO oscillator or from the external clock input. The PXDAC4800 has two clock dividers. Clock divider #1 must be an integer between 1 and 32. Clock divider #2 must be an integer between 1 and 6.

The clock dividers operate in series so that there are 98 unique division combinations for a maximum division of 192. These dividers are also available with an external clock.

The VCO oscillators have extremely low jitter and can be synchronized to an external reference input or to the internal TCXO reference. The internal reference is accurate to better than 3ppm.

Fixed frequency oscillators have been chosen instead of a wide-band frequency synthesizer based on providing an SNR benefit of approximately 10 dB when producing very high frequency output signals.

The PXDAC4800 is a nice complement to Signatec’s PX14400 and PX1500 waveform acquisition boards and is ideal for playing back extremely long waveforms, such as those previously captured with a Signatec Waveform Recording system. This is particularly useful in testing a system’s response to previously recorded real world signals. In such an operation the data is supplied from the high-speed data storage system via the PCI Express bus and the PXDAC4800’s on-board RAM is utilized as a very large FIFO data buffer.

Operating Modes

The PXDAC4800 has 4 operating modes:

- Load RAM
- RAM Playback
- PCIe Streaming Playback
- Standby/Ready

Data Flow

Figure 1 on the following page shows the primary data flow for the PXDAC4800. There is one Virtex-5 FPGA device onboard that handles channel 1 to 4 data flows plus the system PCIe interface and 1 GB memory bank used for storing digital data for conversion to an analog signal.

The System FPGA incorporates the PCI Express Interface and the digital output interfaces for the four DAC channels. Data Flow to the DACs is always supplied via the onboard RAM. In the RAM Playback mode the data has been previously loaded via the Load RAM mode via the PCIe bus. In the PCIe Playback mode the RAM is used as a large FIFO with the data source being the PCIe bus.

Per-trigger Operation

When per-trigger operation is selected, a single trigger, from either the external trigger input or via software, causes a waveform to be generated from a block of RAM. At that point the card is re-armed and is waiting for a new trigger to generate the same block or the next block.

Continuous Looping

When the waveform data source is the on-board RAM, repeating waveforms can be generated by activating the “continuous looping” feature. In this mode the start of the waveform will be at address 0 and the “looping address” is the ending address.

PCIe Playback Mode

Data may be supplied to the DACs as a continuous stream via the PCIe bus. While operating in this mode, data can be sustained from the PC to the board for digital to analog conversion at up to 900 MB/s[1]; 450 MSPS for 14-bit data or 900 MSPS for 8-bit data. In the PCIe Streaming Playback mode, the entire onboard RAM is used to buffer the data against breaks in the signal data (underflow condition). The 1 GB RAM buffer is especially useful since it is of sufficient size to buffer against periodic delays from non real-time operating systems such as Windows.

External Trigger

An external trigger input is provided. The proper signal edge will activate the output from the DAC. This allows the output waveform to be synchronized with an external event.

Clock Generation

Figure 2 on the following page depicts the mechanization of the PXDAC4800 clock circuitry. The DAC clock can be derived from on-board 1200 MHz or 900 MHz VCO oscillators or from an externally supplied clock. If either of the internal oscillators is selected, their outputs will be synchronized to the internal or external 10 MHz reference clock via a phase lock loop. In this case the DAC clocking frequency will have the same accuracy as the reference clock. The internal reference accuracy is better than 3ppm. If used, an external reference clock must have frequency accuracy as stated in the specification section of this data sheet in order to guarantee that the onboard phase lock loop will attain lock.

[1] The maximum speed depends of the PCIe slot type, hard-drive/raid speed, PC internal architecture and chipset.

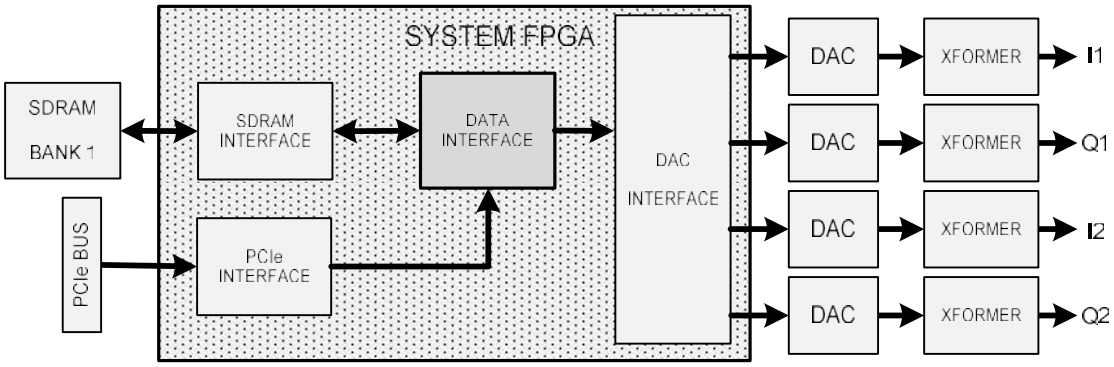


Figure 1 – PXDAC4800 Data Flow

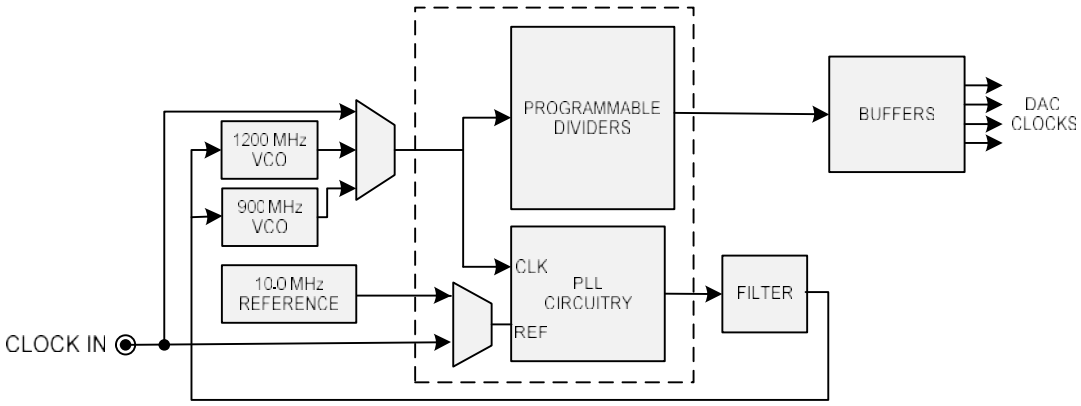
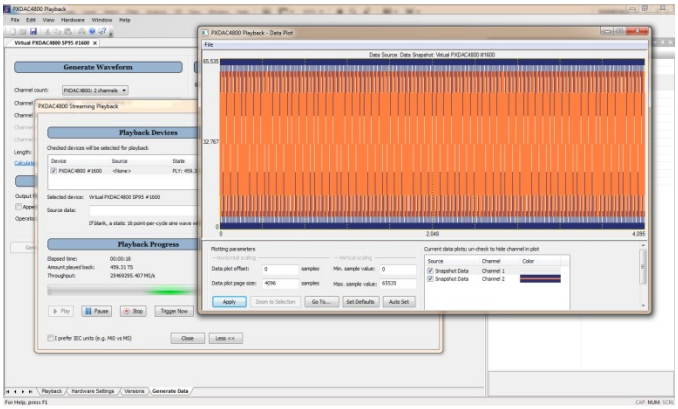


Figure 2 – PXDAC4800 Clock Mechanization

PXDAC4800 Playback Application



The PXDAC4800 Playback Application software is utilized to playback signal data that is loaded in RAM, to playback previously recorded signal data files, and for generating signal data output.

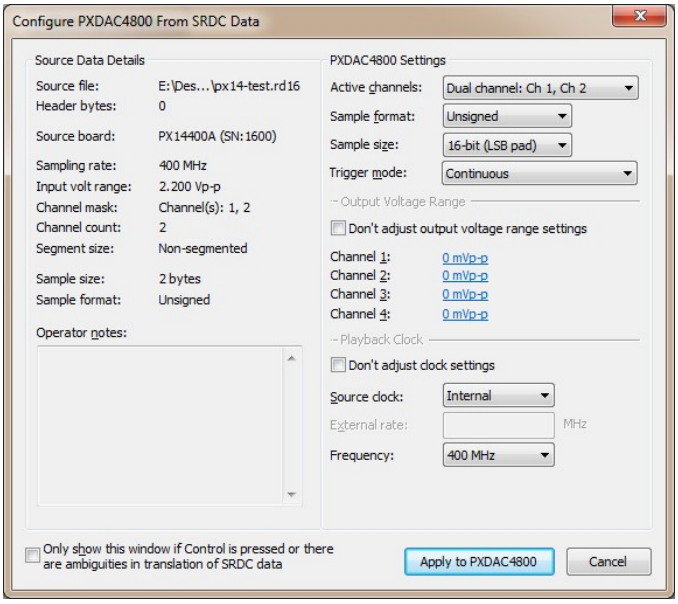
When the Playback Application starts, it will automatically connect to all local PXDAC4800 devices. Note that when the application starts up, the PXDAC4800 hardware is not accessed. This allows the Playback Application to run without directly affecting any operation that may be in progress with other software.

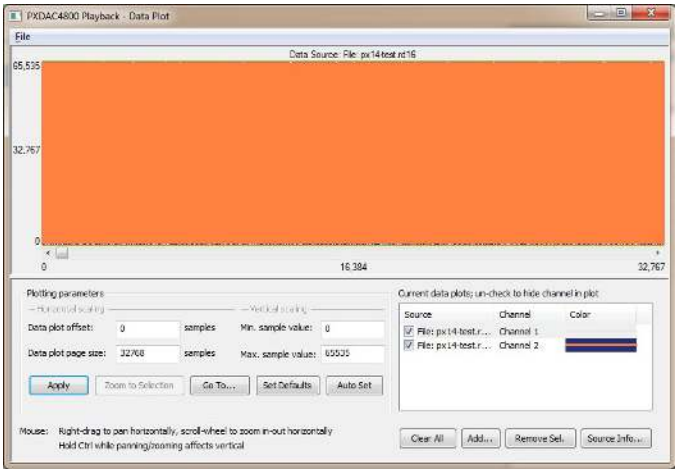
The Playback Application may be used to modify any of the various settings that affect how the generator behaves. These settings are distributed over the tabbed view at the bottom of the main device form. Tabbed settings include:

Playback	Settings for initiating and starting RAM Playback or Streaming File Playback.
Hardware Settings	Settings that control generator output including playback clock, playback channels, playback trigger, output voltage ranges and playback data format.
Versions	Contains an interface to read hardware status items with version and configuration information for various hardware, firmware, and software entities displayed.
Generate Data	Settings for signal waveform generation including number of channels, waveform type and parameters, sample format, and scope data preview.

The PXDAC4800 has two main modes of waveform generation: RAM Playback and Streaming File Playback. When loading or streaming playback data from a file, the Playback Application assumes that the file is raw playback data with no additional context information.

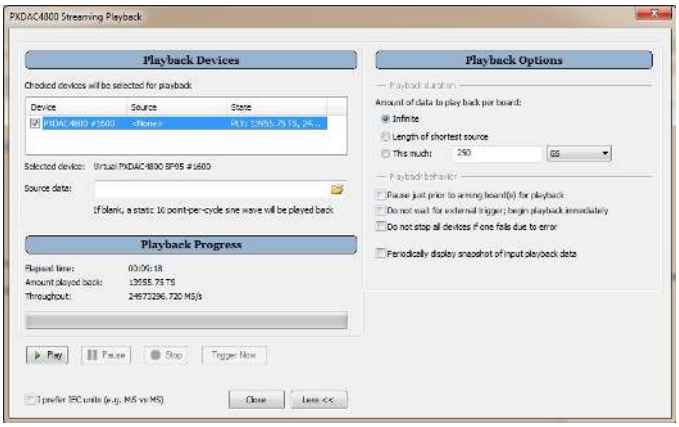
In a RAM Playback operation, the PXDAC4800 plays back data that is currently located in the onboard RAM. On the Playback tab, a data source file can be specified to be loaded for RAM playback. If the specified data source file has an associated Signatec Recorded Data Context (SRDC) file, the SRDC file details can be viewed directly, the actual signal data from the specified source file can be immediately viewed within a scope display, and the hardware settings can be auto-configured from the data with options to modify settings as desired.





The source file can be uploaded with options including upload length and file offset. If the PXDAC4800's RAM length exceeds the source data length, the source data can be looped on a specified RAM offset and RAM length in number of samples. RAM playback can also be started with an option to force a trigger to initiate playback immediately.

In a Streaming File Playback operation, the PXDAC4800 plays back data that is streamed into the board from the host PC. This method is used to playback long records that do not fit in the onboard RAM.

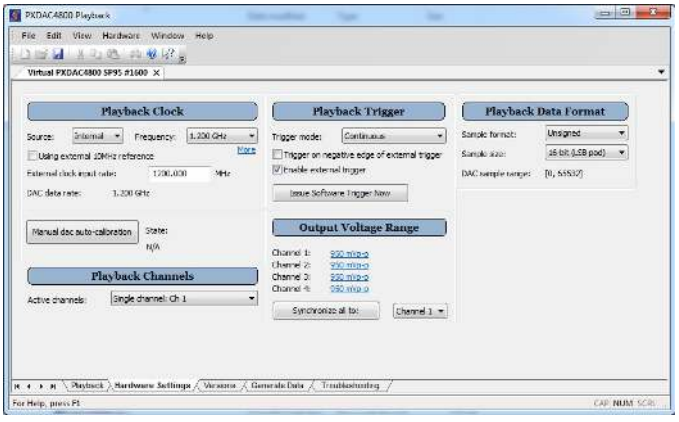


The following playback durations can be specified:

Infinite	Playback goes on indefinitely until manually stopped by the operator.
Length of Shortest Source	Playback will proceed for the length of the shortest source and then stop.
This much (data amount)	Playbacks the amount of data specified in unit of samples, KiS (2^{10} samples), MiS (2^{20} samples), or GiS (2^{30} samples).

Playback statistics are displayed during the live playback detailing the current elapsed time, the amount played back, and the throughput rate.

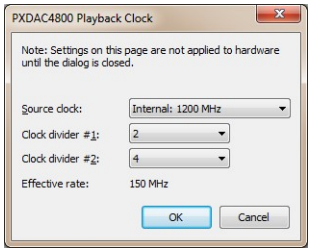
The Playback Application is also used for generating arbitrary waveforms for playback. Various hardware settings can be specified for generating arbitrary waveform output on the Hardware Settings tab.



The playback clock is the clock that is used to drive the onboard digital to analog converters (DACs). With each rising edge of the playback clock, the DAC will output one sample of playback data.

The PXDAC4800 can be configured to use one of several playback clock sources:

Internal Clock	Two oscillators may be used as the playback clock source, a 1200MHz oscillator and a 900MHz oscillator. If the 1200 MHz or 900 MHz oscillator is chosen, it is phase locked to a 10 MHz reference clock which may be the on-board reference or a reference supplied via the clock input.
External Clock	An externally provided clock from the board's external clock input. When using an external clock, the board must be informed of the external clock rate so that it can properly synchronize with the clock.



When either the external clock or one of the internal oscillators is selected as the playback clock source, two clock dividers are available. Clock divider #1 must be an integer between 1 and 32 and divider #2 must be an integer between 1 and 6. These clock dividers operate in series for a 98 unique dividers spanning 1 (no division) to 192.

For Playback Channels, the active channels selection defines which channels will be played back for subsequent playback operations. The PXDAC4800 can support 1, 2, or 4 output channels in various combinations:

Active Channels Selection	Channel Count	Channel Outputs
Quad (Ch. 1, 2, 3, 4)	4	Channels 1, 2, 3, 4
Dual (Ch. 1, 2)	2	Channels 1 and 2
Dual (Ch. 3, 4)	2	Channels 3 and 4
Single (Ch. 1)	1	Channel 1
Single (Ch. 2)	1	Channel 2
Single (Ch. 3)	1	Channel 3
Single (Ch. 4)	1	Channel 4

When the PXDAC4800 is placed into a playback mode, the card will be armed for playback but will not start outputting data until a trigger has been detected. A trigger is an event that is used to synchronize the start of data output to some external event.

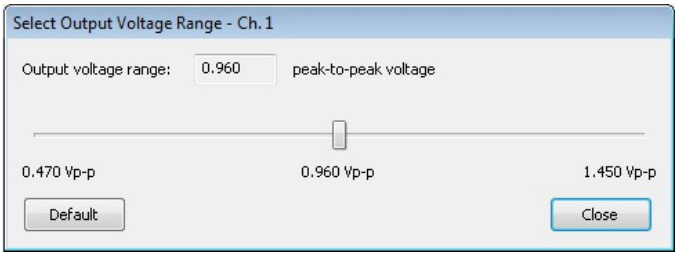
The trigger mode setting is used to select how trigger events are used to start data playback. The PXDAC4800 implements three trigger modes:

Per-trigger	Each trigger event will result in the board playing back a static number of samples (which may be the whole active memory region). The size of this segment is called the Playback Byte count. This trigger mode is not valid for Streaming Playback operations.
Continuous	A single trigger event is used to begin a continuous looping of the playback data. In the case of a RAM playback, when the board gets to the end of the playback data it will loop around back to the start of the playback data and resume playback with that data. This trigger mode is not valid for Streaming Playback operations.
Single Shot	This is a special case of the Per-Trigger mode in which a single trigger event is used to begin playback of a static number of samples. The difference is that only the first trigger is registered and all subsequent triggers are ignored.

When the external trigger is selected as the trigger source, a trigger event is defined by a pulse on the external trigger connector. An external trigger pulse is only considered a trigger event when the card is armed for a playback and waiting for a trigger event. Any trigger pulses that may occur while the card is not waiting for a trigger event will be ignored. The PXDAC4800 can be configured to trigger on the rising edge or falling edge of the external trigger pulse.

The PXDAC4800 can also be explicitly triggered by the software. A software generated trigger can be issued prior to, or while, the card is waiting for a trigger. When the software generated trigger is issued, the board will stop waiting for a trigger event and immediately begin playing back data.

The output voltage range can be specified for each channel from 470mV peak-to-peak to 1450mV peak-to-peak in PXDAC4800A, and from 400mVp-p to 1470mVp-p in PXDAC4800D.



For playback data format, the PXDAC4800 is capable of playing back 8-bit or 14-bit samples (aligned to 16-bits). Further, samples may be either unsigned [0…N] or signed [-N, +N-1].

The following table shows the minimum, midscale, and maximum DAC sample values for the various sample sizes and formats:

	Unsigned			Signed		
	Min.	Mid.	Max.	Min.	Mid.	Max.
14-bit MSB pad	0	8192 (0x2000)	16383 (0x3FFF)	-8192 (0x2000)	0	8191 (0x1FFF)
14-bit LSB pad	0	32768 (0x8000)	65532 (0xFFFC)	-32768 (0x8000)	0	32764 (0x7FFC)
8-bit	0	128 (0x80)	255 (0xFF)	-128 (0x80)	0	127 (0x7F)

For unsigned 14-bit data, a sample value of 0 is equivalent to the minimum output voltage range. A sample value of 65532 is equivalent to the maximum output voltage range. A sample value of 32768 is approximately equivalent to 0V.

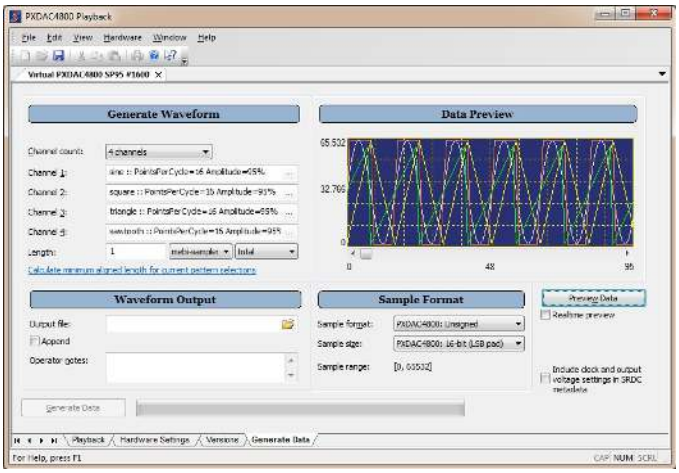
For unsigned 8-bit data, a sample value of 0 is equivalent to the minimum output voltage range. A sample value of 255 is equivalent to the maximum output voltage range. A sample value of 128 is approximately equivalent to 0V.

The PXDAC4800 implements a digital IO interface via the DIG I/O SMA connector on the back of the card. The currently defined Digital Output Modes are as follows:

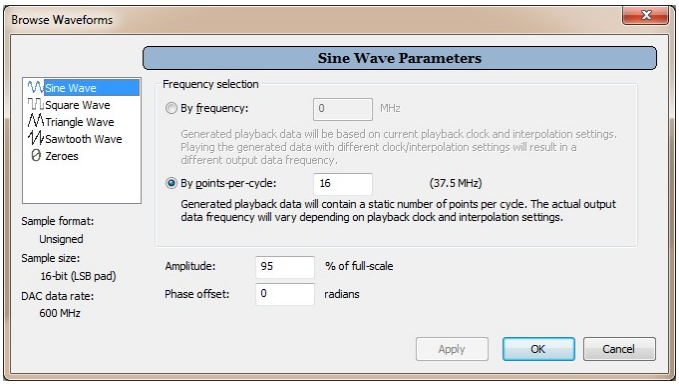
- DATA Clock divided by 8
- Pulse at the beginning of a playback
- Pulse at the end of a playback
- DACs are currently generating data
- Pulse at Underflow error

The Playback Application allows for saving all hardware settings to a file that can be opened and applied to the hardware at a later time, thus saving time from manually re-applying settings for repetitive configurations.

Settings for signal waveform generation including number of channels, waveform type and parameters, sample format, and scope data preview are selected in the Generate Data tab.



A generated waveform pattern can be selected for each output channel that includes sine wave, square wave, triangle wave, sawtooth wave, and zeroes.



For each waveform pattern, the frequency selection can be selected:

By Frequency	An entered frequency value. Generated playback data will be based on current playback clock and interpolation settings. Playing the generated data with different clock/interpolation settings will result in a different output data frequency.
By Points-Per-Cycle	An entered points-per-cycle value. Generated playback data will contain a static number of points per cycle. The actual output data frequency will vary depending on playback clock and interpolation settings.

In addition an amplitude value for % of full scale, a phase offset value in radians and a DC offset value for % of full scale can be specified.

Selecting the Preview Data will then display a preview of the output data results in the preview scope window. The preview scope window is fully interactive so that you can zoom in / zoom out and scroll through the data output results.

The generated waveform output can be saved to an output data file by specifying an output file name. The PXDAC4800 saves multichannel data in a sample interleaved format. This means that each channel is alternated in the output data:

Dual Channel Data Format	Ch. 1 Sample 1, Ch. 2 Sample 1, Ch. 1 Sample 2, Ch. 2 Sample 2, …
Quad Channel Data Format	Ch. 1 Sample 1, Ch. 2 Sample 1, Ch. 3 Sample 1, Ch. 4 Sample 1, Ch. 1 Sample 2, Ch. 2 Sample 2, Ch. 3 Sample 2, Ch. 4 Sample 2, …

It is possible to append an existing output data file if desired. The output data file does not store any context information about the details of the data in the file. The application will automatically generate an associated Signatec Recorded Data Context (SRDC) file for the output data file.

PXDAC4800 Software Libraries

Complete documented Application Programming Interfaces (APIs) with C/C++ callable function libraries for the PXDAC4800 are included for custom software development.

In addition, the complete source code for both the Playback Application is included along with additional project examples that illustrate how to use the function libraries for building custom applications.

LabVIEW interface software is included with supplied LabVIEW virtual instruments (VIs) for the PXDAC4800 with full VI reference documentation for use within the LabVIEW environment

MATLAB interface software is included with supplied MATLAB files (.m) for the PXDAC4800 with full reference documentation for use within the MATLAB environment.

Future manual and software updates are available for download for registered users at no additional charge for the lifetime of the products.

PXDAC4800 SPECIFICATIONS & ORDERING INFORMATION

Signal Connections

DAC Channel 1	: Output
DAC Channel 2	: Output
DAC Channel 3	: Output
DAC Channel 4	: Output
Clock	: Input
Trigger	: Input
Digital I/O	: Input/Output

Connectors

SMA (7 total)

Analog Outputs for PXDAC4800A

Voltage	: 470mV to 1450mV p-p
Impedance	: designed for 50 ohm source
Low Bandwidth (-3dB)	: <2 MHz (tested at 1.2 GSPS)
High Bandwidth (-3dB)	: >400 MHz (tested at 1.2 GSPS)
Coupling	: AC

Analog Outputs for PXDAC4800D

Voltage	: 400mV to 1470mV p-p
Impedance	: designed for 50 ohm source
High Bandwidth (-3dB)	: >590 MHz (tested at 1.2 GSPS)
Coupling	: DC

Analog Performance

	AC		DC	
	10MHz	70MHz	10MHz	70MHz
SNR (dB)	65	61	62	60
THD (dB)	-69	-67	-65	-51
SINAD (dB)	64	60	61	51
SFDR (dB)	73	68	68	51
ENOB+ (bit)	10.2	9.7	9.8	8.2

Test done at 90% of DAC full scale, analog mid-range, 14-bit and 1.2 GHz.
ENOB+ is based on SINAD. Typical results.

External Trigger

Trigger Level	: TTL, CMOS or LVPECL, 3.5V max.
Trigger Input	: 2V comparator with 50mV hysteresis
Coupling	: DC

External Clock

Signal Type	: sine or square wave
Impedance	: 50 ohms to ground
Frequency	: 50 MHz to 1200 MHz
Amplitude	: 500mV p-p to 2.0V p-p
Coupling	: AC

Reference Clock

External

Signal Type	: sine or square wave
Impedance	: 50 ohms to ground
Frequency	: 10.0 MHz ± 200 ppm max.
Amplitude	: 100 mV p-p to 2.0V p-p
Coupling	: AC

Internal

Frequency	: 10.0 MHz ± 3 ppm max.

Trigger Modes

Per-trigger	: single start trigger runs memory data once every trigger
Continuous	: single start trigger runs looped memory data or continuous stream from PCIe bus
Single shot	: single start trigger runs memory data once
Trigger Re-Arm Time	: 16 Clock Cycles

DAC Memory

1 Gigabyte DDR2 SDRAM

Maximum Data Rates

Input Data Rate to each DAC	: 1.2 GSPS
DAC Output Rate	: 1.2 GSPS @ 14-bit for 2 Channels
	: 600 MSPS @ 14-bit for 4 Channels
	: 1.2 GSPS @ 8-bit for 4 Channels
DAC Rise Time	: 800 picoseconds, typical
Jitter Between DAC Inputs	: better than 200 picoseconds
PCIe Bus	: up to 900 MB/s[2]

Power Requirements

+3.3V	: 1.95 Amps max.
+12V	: 1.27 Amps max.

Absolute Maximum Ratings

Trigger Input	: -0.3 to +3.5 volts
Digital I/O	: -0.3 to +3.5 volts
Clock Input	: 5 volts peak to peak
Operation Temperature	: +32°F to +122°F 0°C to +50°C
Storage Temperature	: -4°F to +158°F -20°C to +70°C
Operating Relative Humidity	: 10% to 90%, non-condensing
Board Dimensions	: 6.6" L x 4.4" H x 0.75" W 16.8cm L x 11.1cm H x 1.9cm W

Computer Requirements

I/O Interface	: PCIe x8 Slot
System RAM	: 2 GB for Board Operation 8 GB for PCIe Streaming Operation
Operating System	: Windows 7 (64-bit or 32-bit OS for Board Operation) (64-bit OS for PCIe Streaming Operation)

Ordering Information

Part Number for AC-Coupled = **PXDAC4800A-DP**
Part Number for DC-Coupled = **PXDAC4800D-DP**

Coax Cables

The PXDAC4800 is shipped with four, four foot coaxial cables with SMA connectors on the board end and BNC connectors on the user end. Additional cables may be purchased separately.

Documentation & Accessories

The PXDAC4800 is supplied with a comprehensive Operators Manual that thoroughly describes the operation of the hardware and the software, as well as an appropriate software disk including the SDK (C, LabVIEW and MATLAB).

Product Warranty

All Signatec products carry a standard full 2-year warranty. During the warranty period, DynamicSignals will repair or replace any defective product at no cost to the customer. Warranties do not cover customer misuse or abuse of the products.

Signatec is a product brand of
DynamicSignals LLC, an ISO 9001:2008 Certified Company

Data Sheet Revision 2.1 – 04/05/2016
Specifications are subject to change without notice.

[2] The maximum speed depends of the PCIe slot type, hard-drive/raid speed, PC internal architecture and chipset.